CLAIMS

I/We claim:

1. A resolver circuit comprising:

a signal generation circuit configured to generate an excitation signal;

a bridge tied load amplifier, having an input in electrical communication with the signal generation circuit;

a resolver having an excitation winding in electrical communication with the bridge tied load amplifier;

a resolver processing circuit in electrical communication with a first output winding of the resolver.

2. The resolver circuit according to claim 1, wherein the bridge tied load amplifier has a positive output and a negative output, the positive output being connected to one side of the excitation winding, the negative side being connected to the opposite side of the excitation winding.

3. The resolver circuit according to claim 1, wherein the signal generation circuit is configured to generate a sinewave excitation signal.

4. The resolver circuit according to claim 1, wherein the signal generation circuit is configured to generate an excitation signal of about 10 kHz.

5. The resolver circuit according to claim 1, further comprising a low pass filter connected between the signal generation circuit and the bridge tied load amplifier.

6. The resolver circuit according to claim 1, wherein the low pass filter includes a resistive load in electrical series with the bridge tied load amplifier and a capacitive load electrically parallel with the bridge tied load amplifier.

7. The resolver circuit according to claim 1, wherein the resolver includes a second output winding an electrical communication with the resolver processing circuit.

8. The resolver circuit according to claim 1, wherein the signal generation circuit and the resolver processing circuit form portions of a single integrated circuit device.

9. The resolver circuit according to claim 1, wherein the bridge tied load amplifier includes a first linear amplifier and a second linear amplifier.

10. The resolver circuit according to claim 1, wherein the first and second linear amplifiers have an output offset voltage at half the supply voltage.

11. The resolver circuit according to claim 1, wherein the second linear amplifier has an inverted output in communication with a negative output of the bridge tied load amplifier.